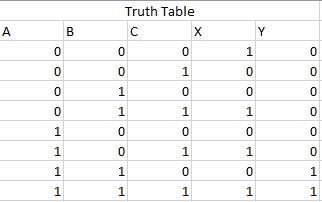
M Ahmed Naveed 2022-EE-168

**Digital System**

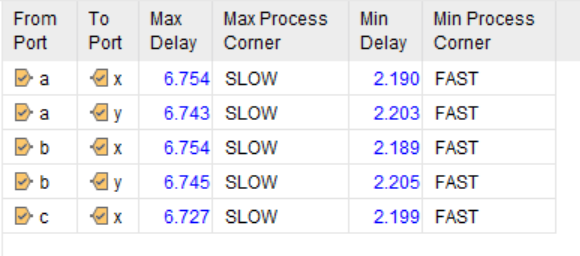
Experiment 3

Combinational Circuits: Structural Modeling Simulation using Vivado

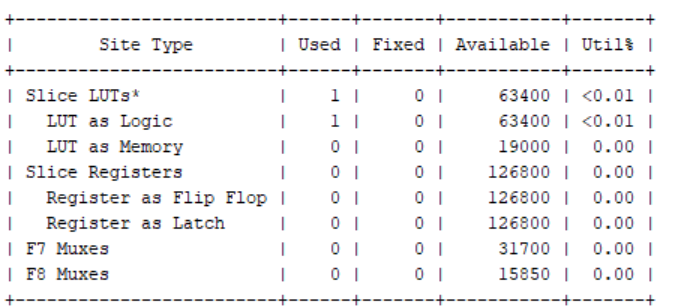
Truth table

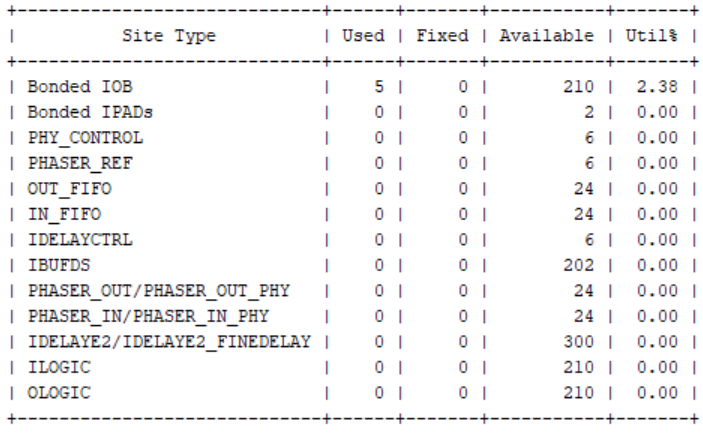


Maximum combinational delay:



Resource utilization:





S

System Verilog Code:

module alab3(

input logic a,

input logic b,

input logic c,

output logic x,

output logic y

);

logic p, q, r, s, t;

assign p = ~c;

ssign q = a | b;

assign r = ~(a & b);

assign s = a | b;

assign t = r ^ s;

assign x = p ^ q;

assign y = q&t;

endmodule